# A Circuit-Based Approach to Efficient Enumeration

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[2]CNRS CRIStAL

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[4]CNRS CRIL

# Problem statement

# Problem: Enumerating large result sets

Input

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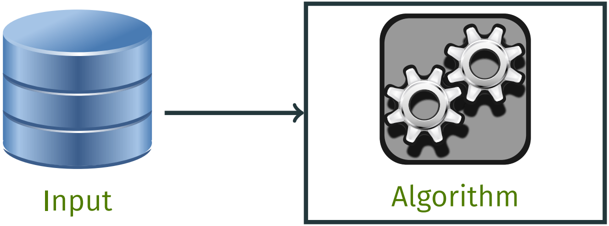

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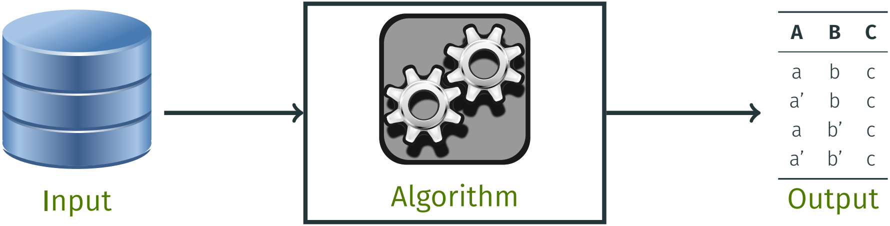


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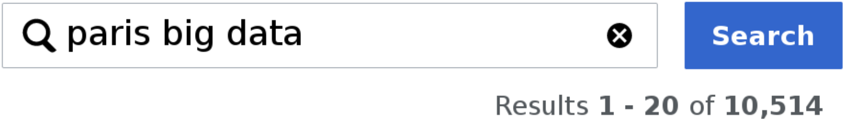

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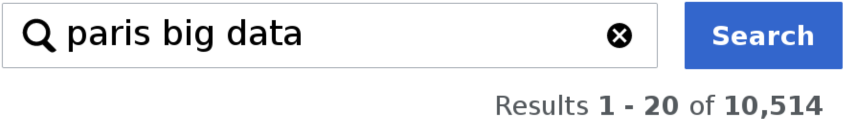


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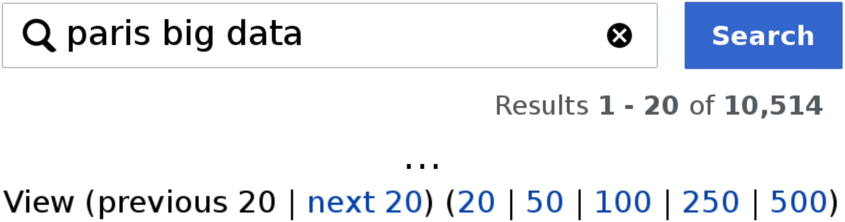

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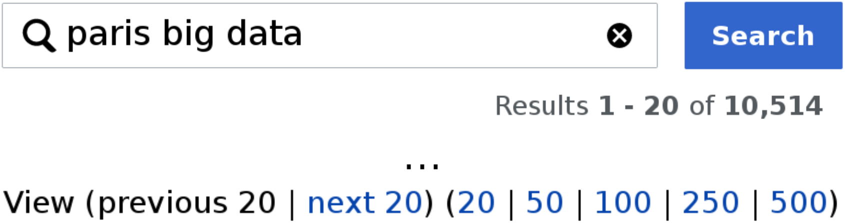


→ Solution: Enumerate solutions one after the other

# Enumeration algorithm

Input

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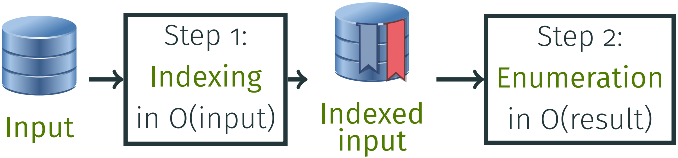

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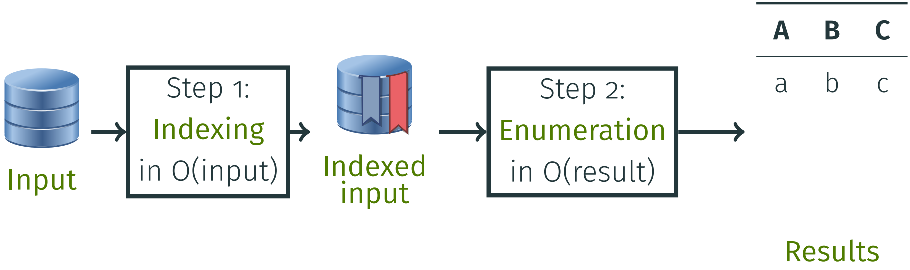

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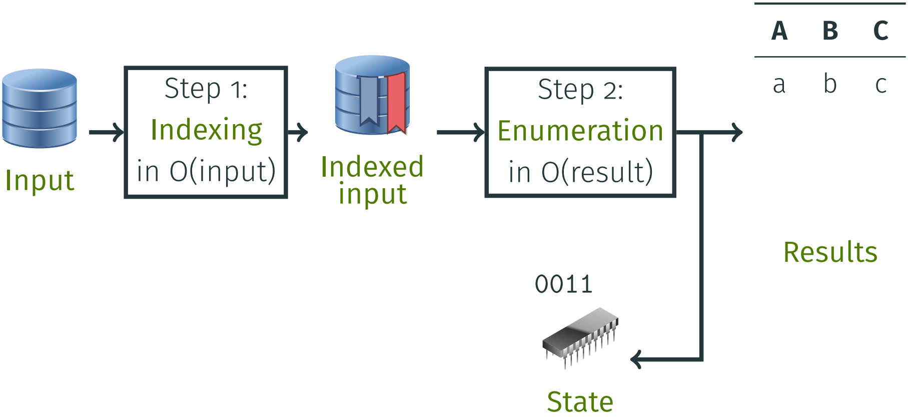

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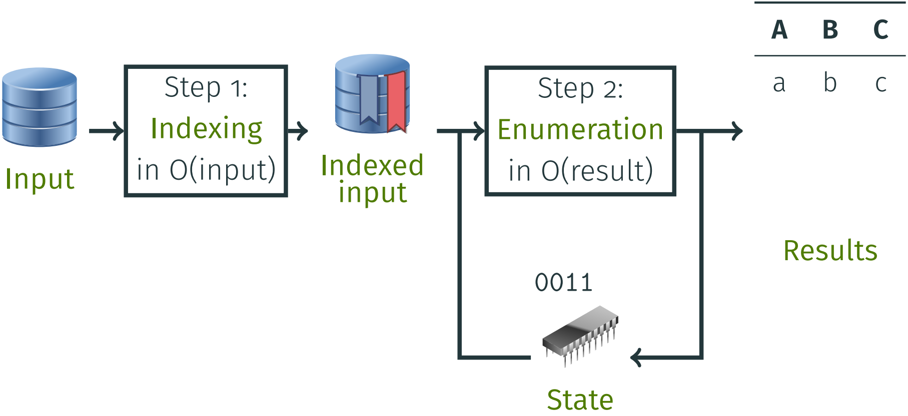

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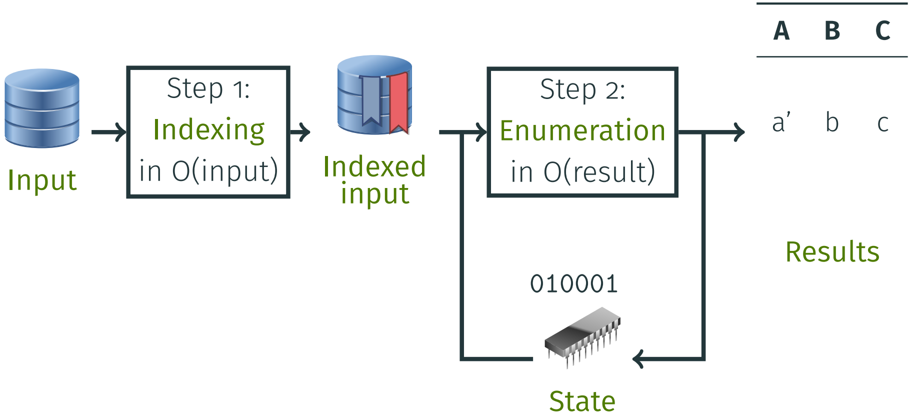

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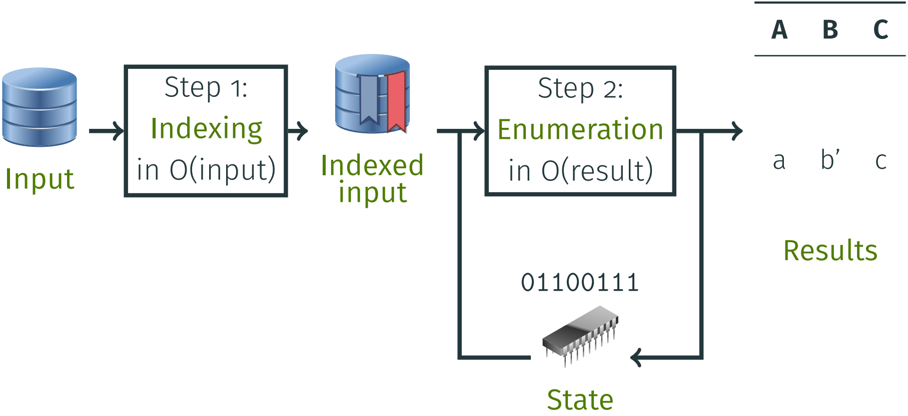

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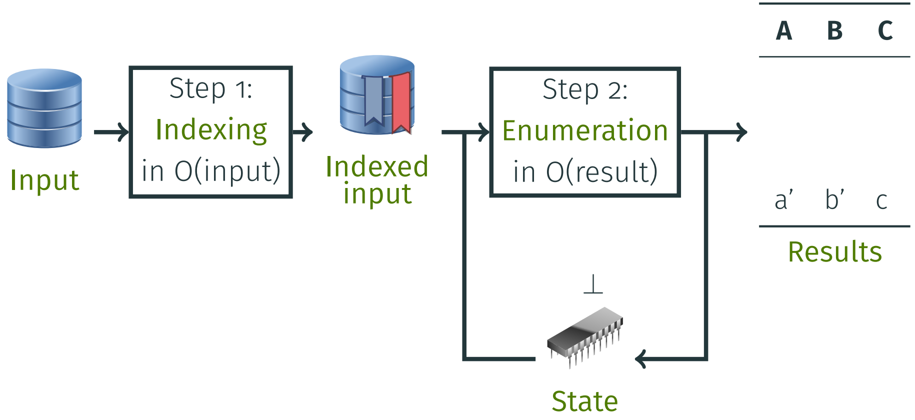

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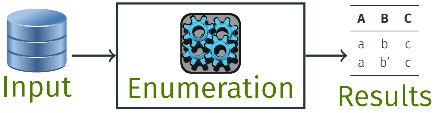

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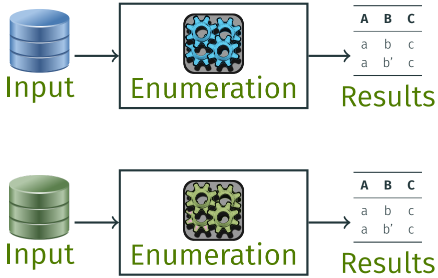

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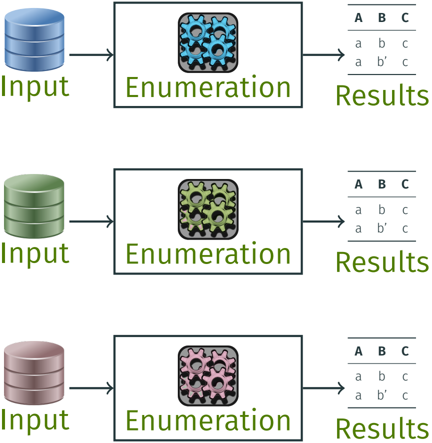

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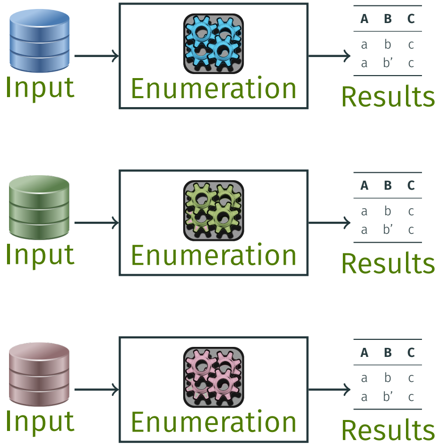


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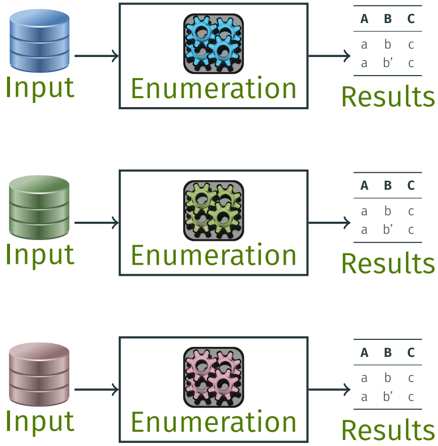


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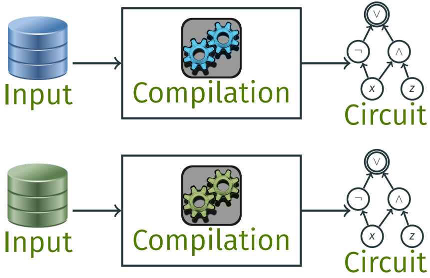

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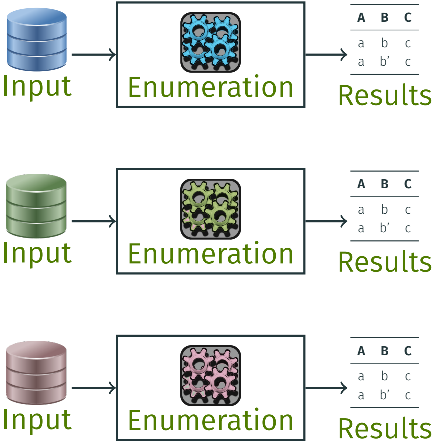


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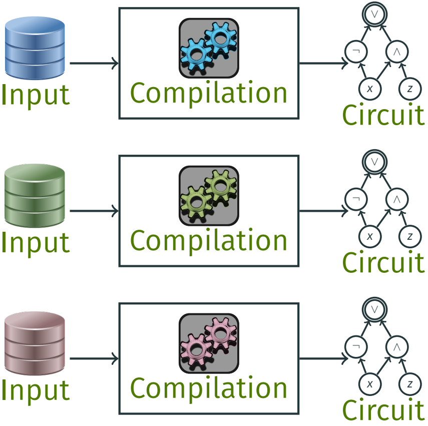

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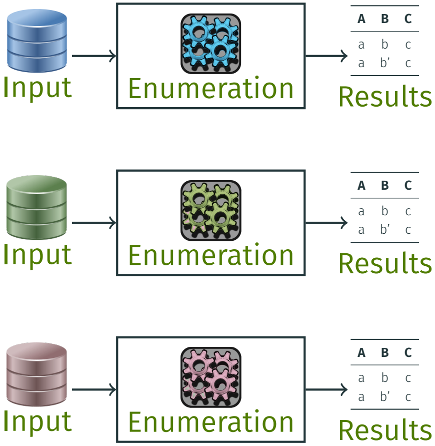


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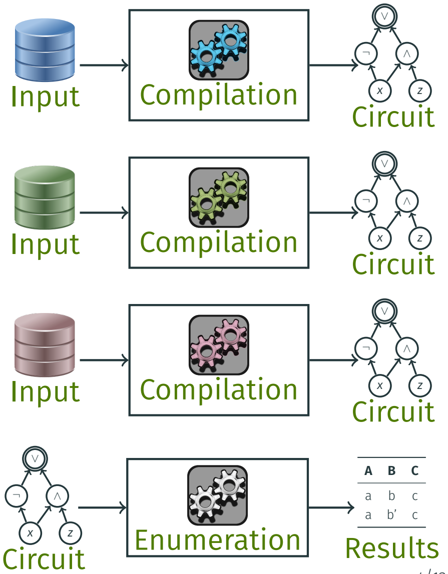
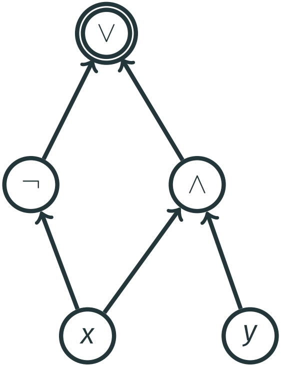


## Boolean circuits




- Directed acyclic graph of gates

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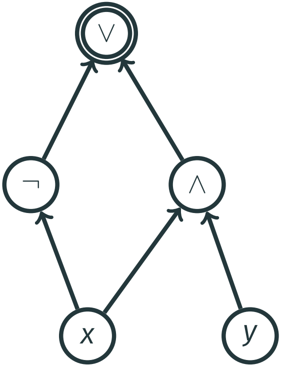


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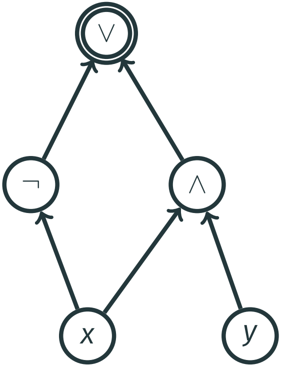


- Directed acyclic graph of **gates**
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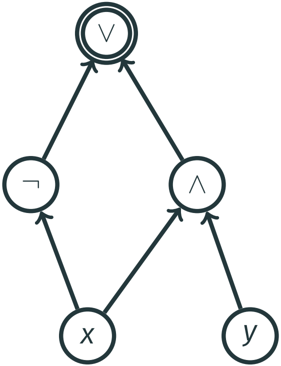


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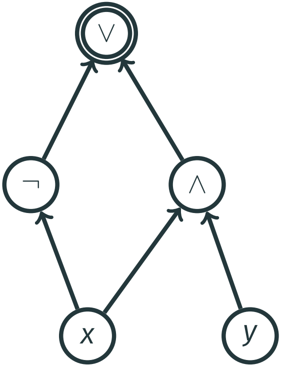


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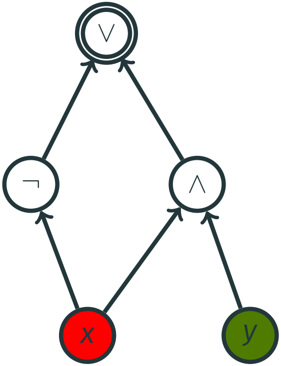


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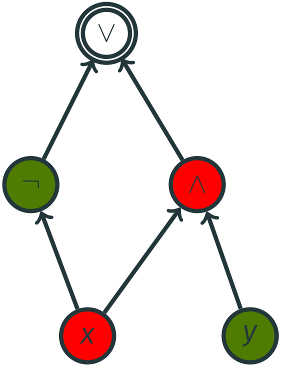


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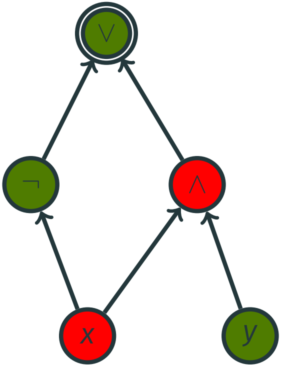


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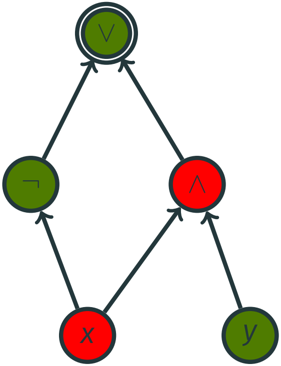


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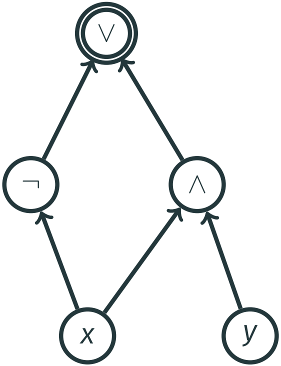


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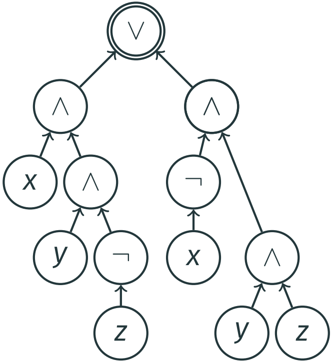
**Our task:** Enumerate all **satisfying assignments** of an input circuit

# Circuit restrictions

**d-DNNF:**

- $\vee$ are all deterministic:

The inputs are mutually exclusive (= no valuation $\nu$ makes two inputs simultaneously evaluate to 1)



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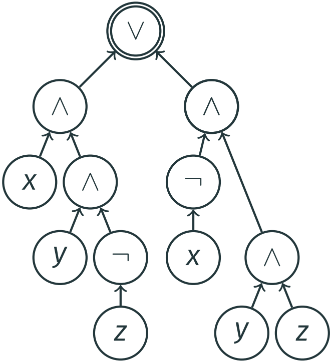

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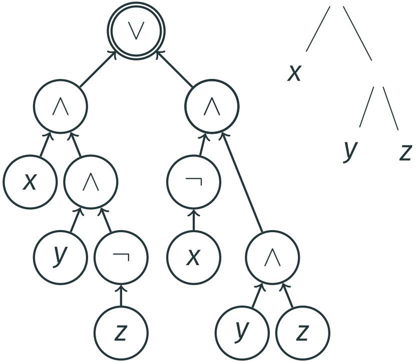
**v-tree:** $\wedge$-gates follow a tree on the variables



# Main results

**Theorem**

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Also: restrict to assignments of constant size $k \in \mathbb{N}$ (at most $k$ variables are set to $1$):

**Theorem**

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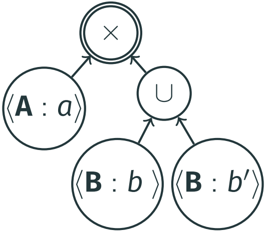

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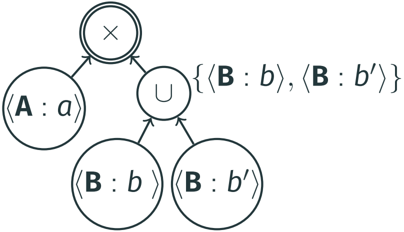

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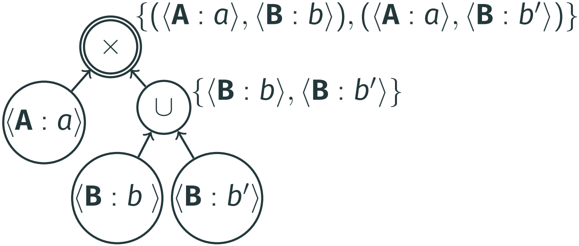

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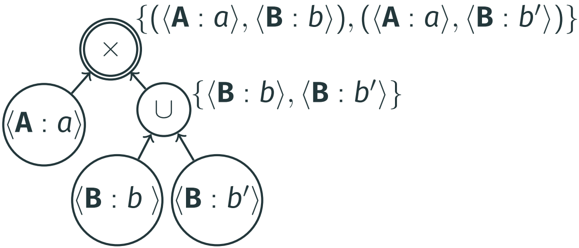


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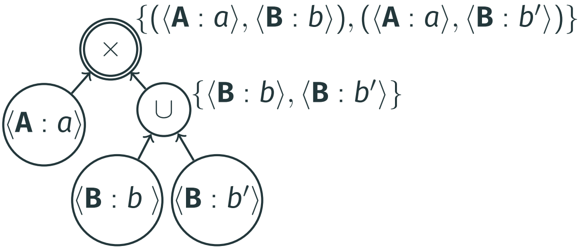


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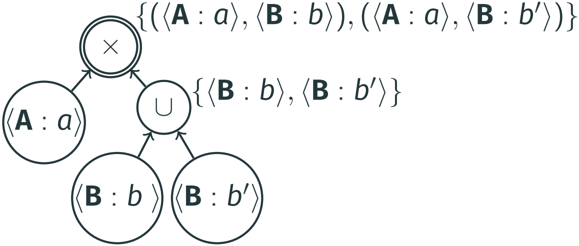


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**Theorem (Strenghtens result of [Olteanu and Závodnỳ, 2015])**
*Given a deterministic factorized representation, we can enumerate its tuples with linear preprocessing and constant delay*

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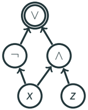
**Theorem (Recaptures [Bagan, 2006], [Kazana and Segoufin, 2013])**
*Given a MSO query $Q$ and a database $D$, the results of $Q$ on $D$ can be enumerated with linear preprocessing in $D$ and linear delay in each answer ($\rightarrow$ constant delay for free first-order variables)*

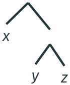
# Proof techniques

# Proof overview

## Preprocessing phase:




Circuit




v-tree

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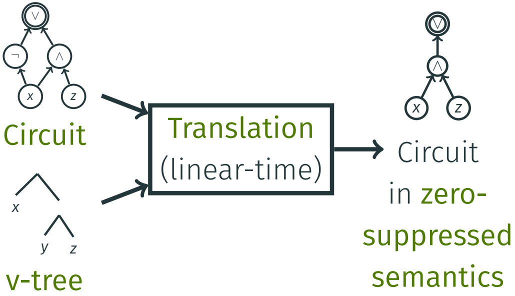

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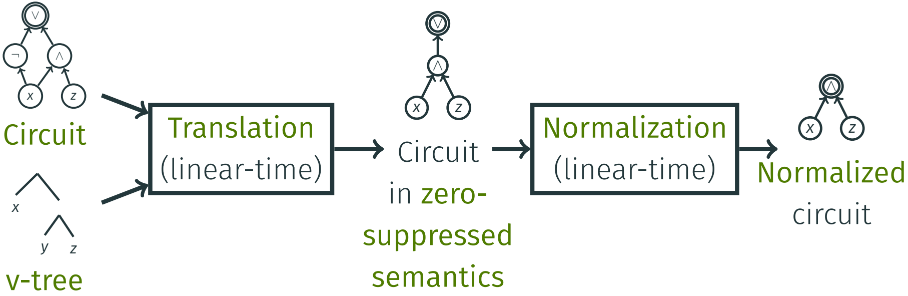

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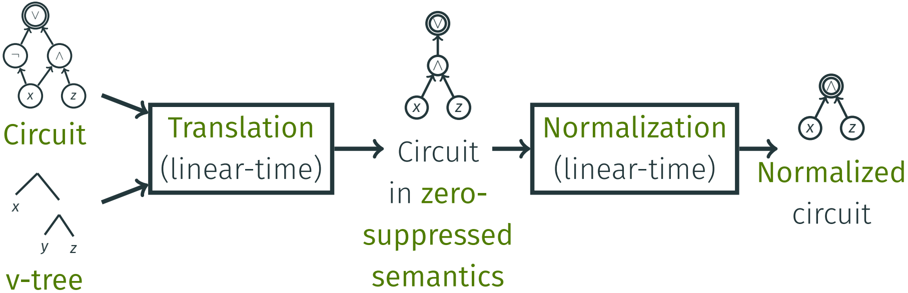
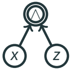


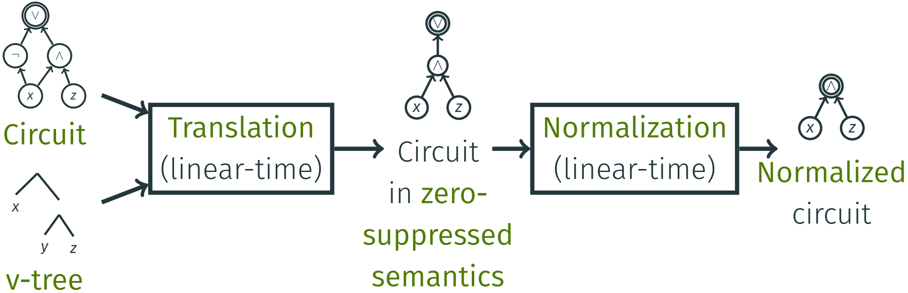

## Enumeration phase:



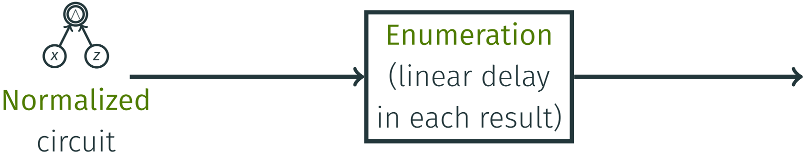

Normalized
circuit

# Proof overview

## Preprocessing phase:



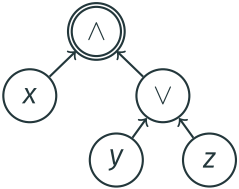

## Enumeration phase:




| A | B | C |
|---|---|---|
| a | b | c |
| a | b’ | c |

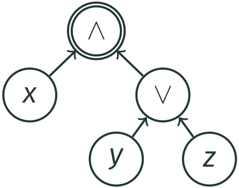
Results

# Zero-suppressed semantics




Special zero-suppressed semantics for circuits:

# Zero-suppressed semantics




Special zero-suppressed semantics for circuits:

- No NOT-gate
- Each gate captures a set of assignments
- Bottom-up definition with $\times$ and $\cup$

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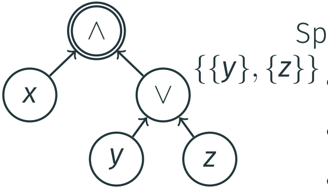


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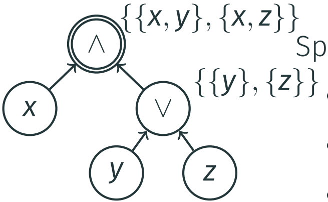


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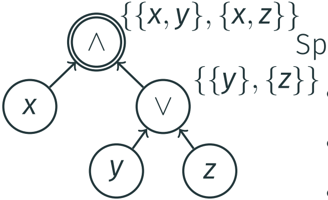


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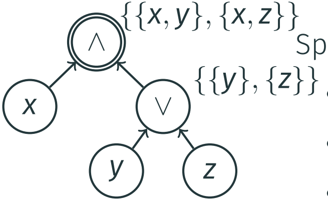


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Many equivalent ways to understand this:

- Generalization of factorized representations
- Analogue of zero-suppressed OBDDs (implicit negation)
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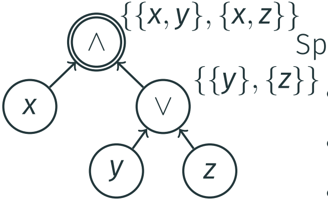


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Simplification: rewrite circuits to arity-two (fan-in $\leq 2$)

# Enumerating assignments in the zero-suppressed semantics

Task: Enumerate the elements of the set $S(g)$ captured by a gate $g$

→ E.g., for $S(g) = \{\{x, y\}, \{x, z\}\}$, enumerate $\{x, y\}$ and then $\{x, z\}$

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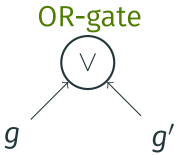


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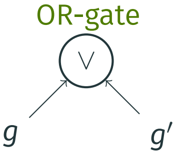


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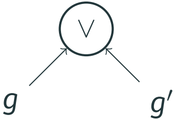
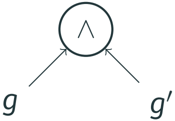



AND-gate

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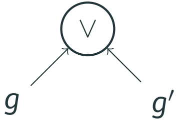


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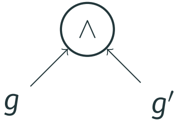


Lexicographic product: enumerate $S(g)$ and for each result $t$ enumerate $S(g')$ and concatenate $t$ with each result

Decomposability: no duplicates

# Conclusion

## Summary and conclusion

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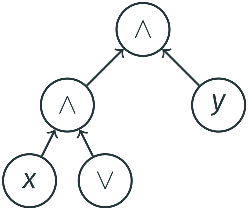
Thanks for your attention!

# Normalization: handling $\emptyset$



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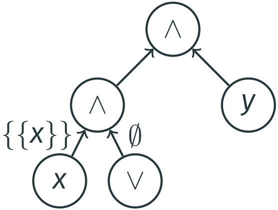

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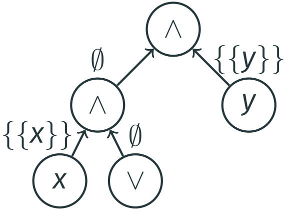

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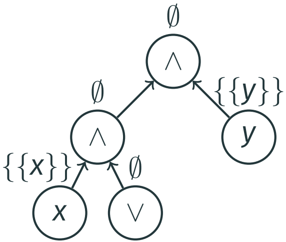

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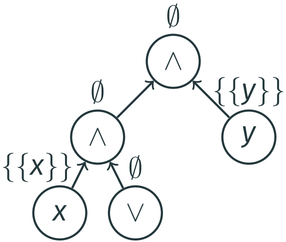


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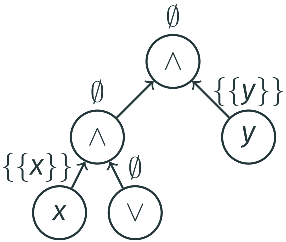


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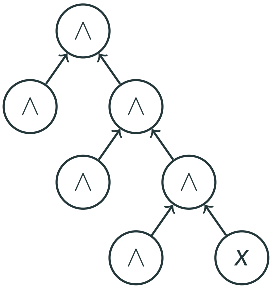

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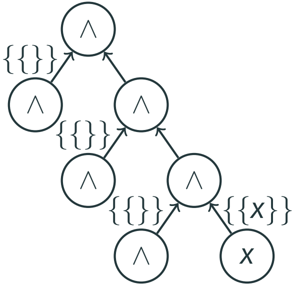

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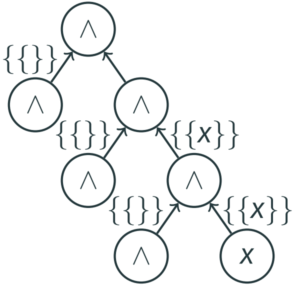

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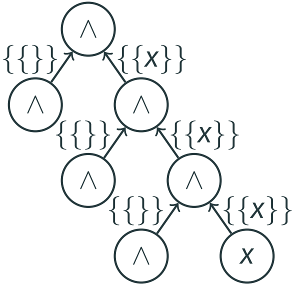

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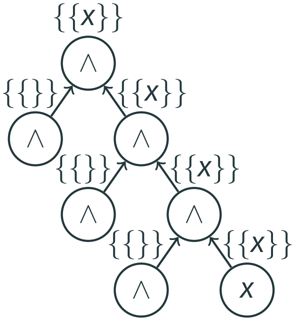

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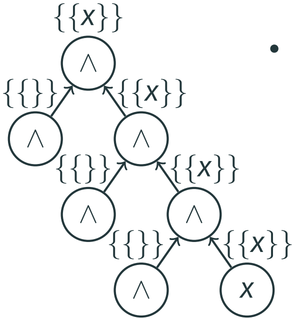


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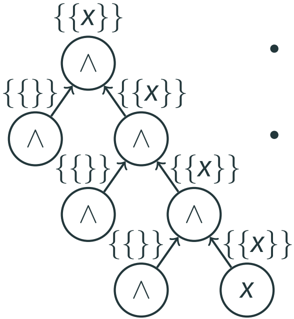


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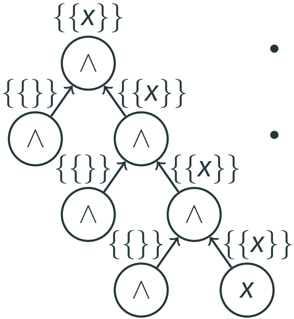


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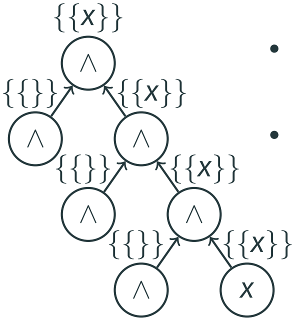


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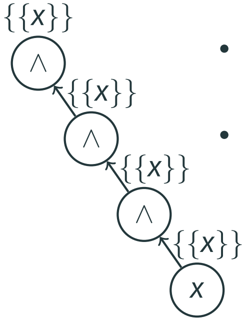


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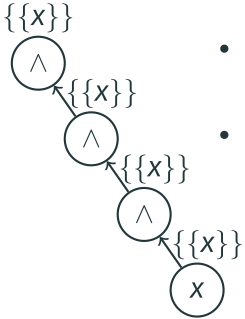


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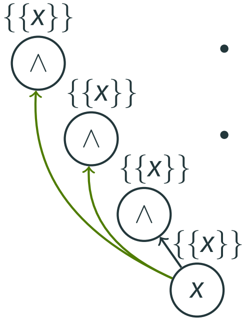


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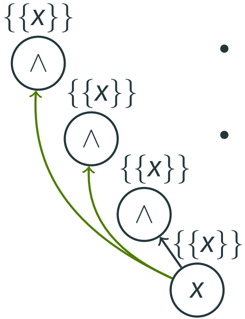


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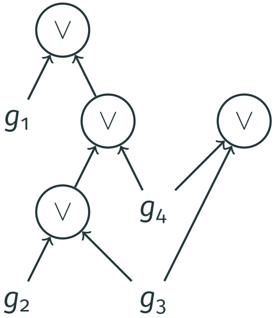
$\rightarrow$ Now, traversing an AND-gate ensures that we make progress: it splits the assignments non-trivially

# Normalization: handling OR-hierarchies

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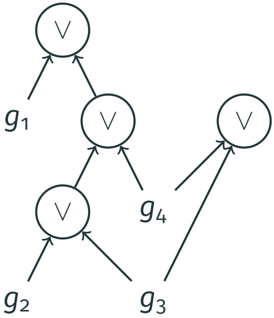


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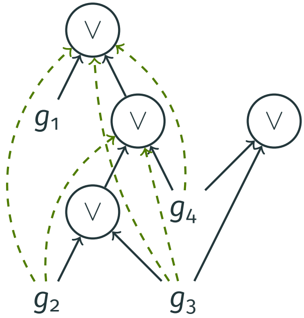


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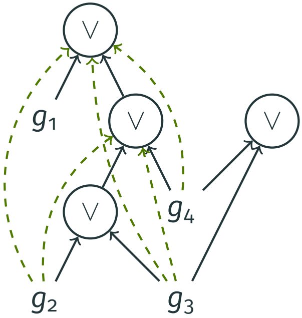


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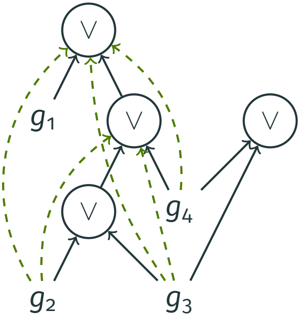


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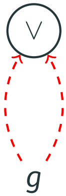
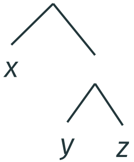
Solution:

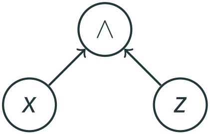
- **Determinism** ensures we have a **multitree** (we cannot have the pattern at the right)
- **Custom** constant-delay reachability index for multitrees



# Translating to zero-suppressed semantics

- This is where we use the v-tree



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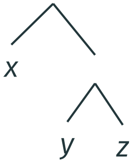


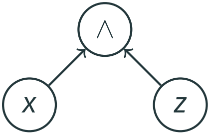

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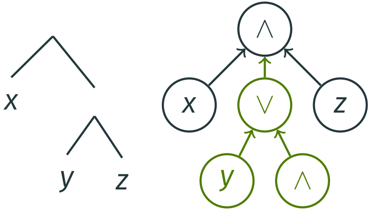

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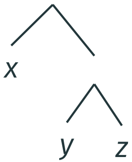


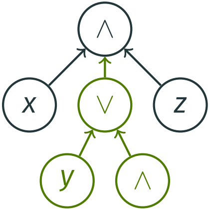


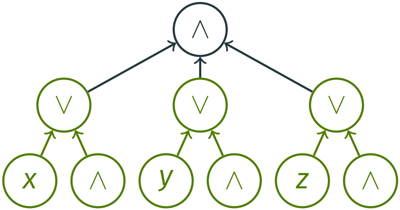


- **Problem:** quadratic blowup

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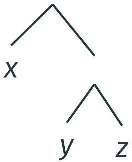
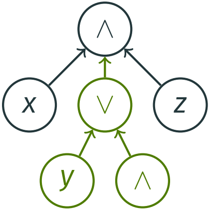
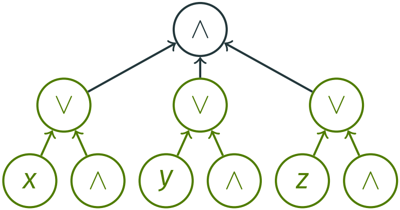
- This is where we use the **v-tree**
- Add explicitly **untested variables**




- **Problem:** quadratic blowup
- **Solution:**
  - **Order** $<$ on variables in the v-tree ($x < y < z$)
  - **Interval** $[x, z]$
  - **Range gates** to denote $\bigvee[x, z]$ in constant space

# References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